Project 3 Audio Equalizer

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Abstract

This experiment aim was to design an audio equalizer in accordance with specific constraints. Key objectives include implementing low-pass, mid-pass, and high-pass filters with individual volume controls. Additional goals include achieving V_{amp} values at minimum and maximum settings, maintaining a maximum ripple of 15 mV_{rms}, and ensuring an output power greater than 400 mW for all frequencies. The approach involved breaking down the complete circuit into smaller elements before integration.

The findings show the low-pass, mid-pass, and high-pass filters are close to the theoretical cutoff frequencies. V_{amp} testing demonstrated effective volume control across various frequencies. However, a shortcoming was identified as the circuit failed to meet the maximum V_{amp} requirement at 200 Hz and 2000 Hz, where DC RMS voltages exceeded the 10% error margin. A potential reason is due to the capacitor selection in the low-pass filter.

Overall, the experiment was largely achieved. The completion of an audio equalizer with functional filters, volume controls, and power amplification. Despite minor errors in the maximum V_{amp} requirements, the overall performance of the circuit was acceptable. If the circuit was to be constructed in the future, adjustments to component values would be considered.

1. Objectives

The overall object of this experiment is to design and create an audio equalizer. For the audio equalizer, several constraints were given. As shown in Figure 1.1, these are the constraints that must be met for the audio equalizer.

Specification	Requirement
Speaker Impedance	8 Ohm
Bass filter -3dB cutoff	320Hz $\pm$10%
Mid filter -3dB cutoffs	320-3200Hz $\pm$10%
Treble filter -3dB cutoff	3200Hz $\pm$10%
V_{amp} with all volumes turned to minimum settings	$<15mV_{RMS}$ @ 100 Hz, 1000 Hz, 10000 Hz
V_{amp} with all volumes turned to maximum settings	100 mV_{RMS} $\pm$ 10% @ 100 Hz, 1000 Hz, 10000 Hz
Maximum ripple	$15mV_{rms}$
Output power	Greater than 400 mW from 100 Hz to 10000 Hz

Figure 1.1: Specification and Requirements for the Specifications of the Audio Equalizer.

2. Theory

This experiment calls for the utilization of a low-pass, mid-pass, and high-pass filter. This is because of the need to separate the different frequencies that are passing through the circuit. Each frequencies needs to be separated because of the requirement to be able to control the different volumes at each frequency. Thus, a low-pass filter, a mid-pass filter, and a high-pass filter are needed with their own volume control.

To wire a low-pass filter, please see Figure 2.1. To wire a high-pass filter, please see Figure 2.2. The RC filter equation that is used to calculate the frequency for the cutoff is shown in Equation 1, which is used for both the low-pass filter and high-pass filter.

A mid-pass filter is different from a low-pass filter and a high-pass filter. This is because of the need to prevent a certain range of low frequencies as well as prevent a certain range of high frequencies. In this is the case a mid-pass filter is essentially a combination of both a low-pass filter and a high-pass filter. However, the series combination of a low-pass filter and a high-pass filter can form positive feedback which can cause a problem, thus the utilization of a buffer between the two is needed. A buffer is the simplest form of negative feedback, where the output voltage is directly attached to the verting input of an op-amp. The wiring of a buffer can be seen in Figure 2.3.

$$f = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi fC} \quad (1)$$

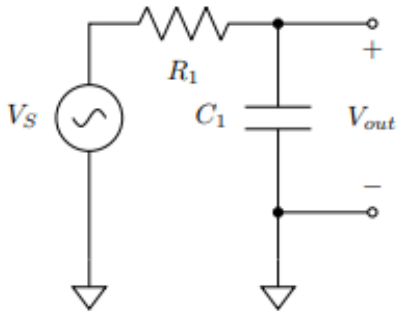

Figure 2.1: RC Low-Pass Filter.

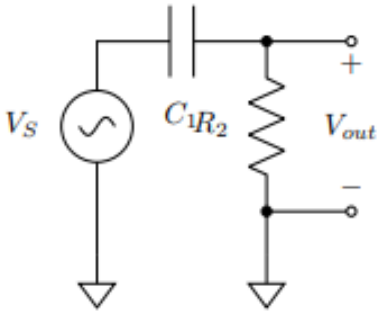

Figure 2.2: RC High-Pass Filter.

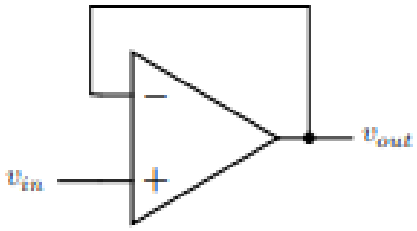

Figure 2.3: Buffer Circuit.

With each of the different filters, they also need to be able to be controlled. This control would be done through the use of an inverting amplifier with a manual control. The way that an inverting amplifier works is by having a voltage divider control that is used to control the voltage that is traveling through the op-amp. This can be seen in Figure 2.4. Additionally, a op-amp changes the gain of the circuit. The gain is calculated by the ratio between the voltage out of the op-amp by the voltage input into the circuit. It can also be expressed by the negative ratio between the resistance that is used to connect the negative input to the output by the resistance used before entering the op-amp. These equations can be seen in Equation 2.

$$Gain = \frac{Vout}{Vin} = -\frac{R2}{R1} \tag{2}$$

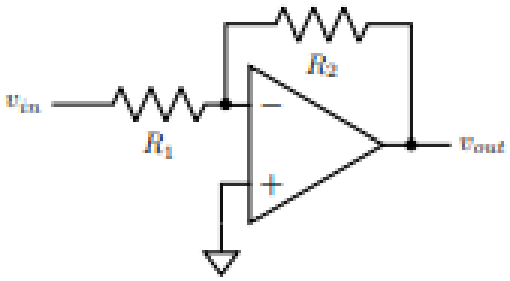

Figure 2.4: Inverting Amplifier.

A few extra equations that are needed for this experiment include the conversion between a standard AC voltage into a RMS voltage. This can be seen in Equation 3..

$$V_{RMS} = \frac{V}{\sqrt{2}} \tag{3}$$

When calculating power, it is the voltage into the component multiplied by the current that is traveling into the component. With is also equal to the voltage squared into the component divided by the resistance the component possesses. This equation can be seen in Equation 4

$$\text{Power} = VI = \frac{V^2}{R} => V = \sqrt{PR} \tag{4}$$

3. Procedure

a. Filters

i. Low-Pass Filter

To be able to isolate the bass frequencies that come into the circuit, a low-pass filter is needed. The low-pass filter circuit shown in Figure 3.1.1 was constructed a RC low-pass filter with a cutoff at 320 Hz. The low-pass filter was constructed utilizing a 4.7 kΩ resistor with a 0.1 µF capacitor.

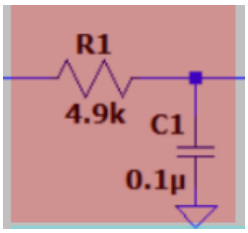

Figure 3.1.1: Low-Pass Filter Circuit Schematic.

Due to there being a very limited number of inductors, an RC low-pass filter was selected to be used. This is because there were more options for capacitors. To select the capacitor and resistor to use, Equation 1 was used. The frequency cutoff for the high-pass was given to be 320 Hz. This means any frequency lower than 320 Hz can pass through the filter, but anything greater cannot. Additionally, there are more resistors than capacitors so a capacitor that provided a resistance that is close to what is given within my kit was selected. The capacitor selected was 0.1 µF, resulting in the resistance being 4.9 kΩ ideally. However, there was no 4.9 kΩ resistor within my kit so a 4.7 kΩ was used instead.

$$R_1 = \frac{1}{2\pi f C} = \frac{1}{2\pi(320\ Hz)(0.1\mu F)} \approx 4.9\ k\Omega$$

ii. High-Pass Filter

To be able to isolate the treble frequencies that come into the circuit, a high-pass filter is needed. The high-pass filter circuit shown in Figure 3.1.2 was constructed a RC high-pass filter with a cutoff at 3200 Hz. The high-pass filter was constructed utilizing a 4.7 kΩ resistor with a 0.01 µF capacitor.

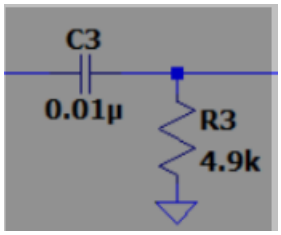

Figure 3.1.2: High-Pass Filter Circuit Schematic.

Due to there being a very limited number of inductors, an RC high-pass filter was selected to be used. This is because there were more options for capacitors. To select the capacitor and resistor to use, Equation 1 was used. The frequency cutoff for the high-pass was given to be 3200 Hz. This means any frequency higher than 3200 Hz can pass through the filter, but anything less cannot. Additionally, there are more resistors than capacitors so a capacitor that

provided a resistance that is close to what is given within my kit was selected. The capacitor selected was 0.01 µF, resulting in the resistance being 4.9 kΩ ideally. However, there was no 4.9 kΩ resistor within my kit so a 4.7 kΩ was used instead.

$$R_3 = \frac{1}{2\pi f C} = \frac{1}{2\pi(3200\ Hz)(0.01\mu F)} \approx 4.9\ k\Omega$$

iii. Mid-Pass Filter

To be able to isolate the middle frequencies that come into the circuit, a mid-pass filter is needed. The mid-pass filter circuit shown in Figure 3.1.3 was constructed utilizing a RC low-pass filter with a cutoff at 3200 Hz, a RC high-pass filter with a cutoff at 320 Hz, and a buffer to prevent positive feedback. The low-pass filter was constructed utilizing a 4.7 kΩ resistor with a 0.01 µF capacitor. The high-pass filter was constructed utilizing a 4.7 kΩ resistor with a 0.1 µF capacitor. The buffer was positioned between the two filters to prevent positive feedback from being created. A LM324 chip was used for the buffer. A +8 V and a -8 V travel through the LM324 with the voltages having a capacitor in parallel being grounded to prevent static from being amplified.

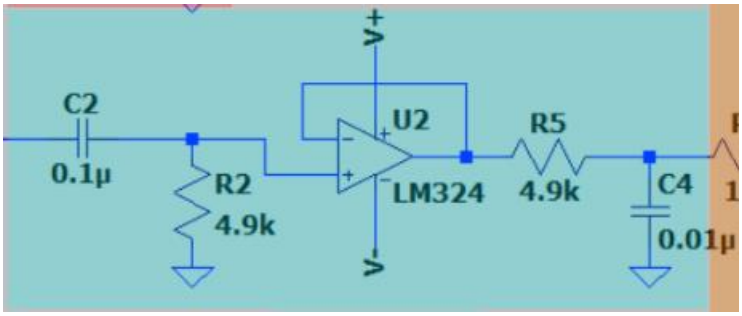

Figure 3.1.3: Mid-Pass Filter Circuit Schematic.

Due to the low-pass having a cutoff at 320 Hz and the high-pass filter having a cutoff at 3200 Hz, the mid-pass needs to share those cutoffs to prevent there from being a gap in the frequencies being filtered. Although the mid-pass filter is a combination of a high-pass and low-pass filter, the frequencies for the cutoffs are slightly different. If the frequency for the low-pass filter was 320 Hz and the high-pass filter was 3200 Hz, the gain would be way less than -3 dB. To fix this and to keep the same cutoff frequencies, simply flip the frequency cutoffs for the two filters. The low-pass filter should have a cutoff frequency of 3200 Hz and the high-pass filter should have a cutoff frequency of 320 Hz.

There are more resistors than capacitors so a capacitor that provided a resistance that is close to what is given within my kit was selected. The capacitor selected for the low-pass was 0.01 µF. The capacitor selected for the high-pass was 0.1 µF. After utilizing Equation 1, the ideal resistance value was found to be 4.9 kΩ for both. However, there are no 4.9 kΩ resistors, the closest one is 4.7 kΩ.

$$R_2 = \frac{1}{2\pi f C} = \frac{1}{2\pi(320\ Hz)(0.1\mu F)} \approx 4.9\ k\Omega$$

$$R_5 = \frac{1}{2\pi f C} = \frac{1}{2\pi(3200\ Hz)(0.01\mu F)} \approx 4.9\ k\Omega$$

b. Filter Voltage Control

After the frequency travels through the different filters, the ability to control the volume of the different frequencies is then needed. Each of the frequency filters have the same volume controller wiring. The volume control circuit shown in Figure 3.2.1 was constructed utilizing an LM324 chip with a 10 kΩ initial resistance with a 10 kΩ potentiometer to control the gain of the op-amp for the second resistor. A +8 V and a -8 V travel through each LM324 with the voltages having a capacitor in parallel being grounded to prevent static from being amplified.

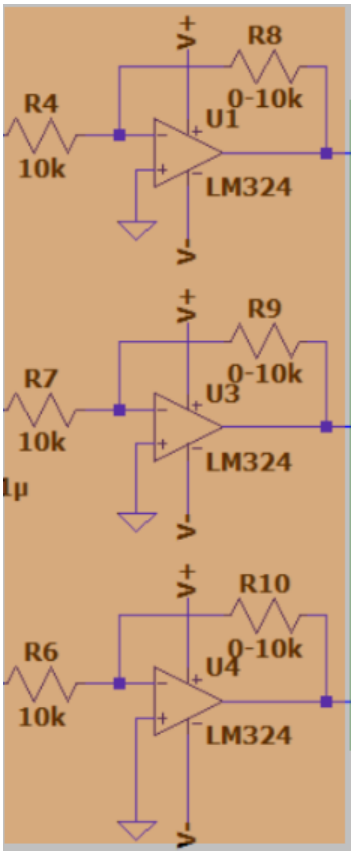

Figure 3.2.1: Filter Volume Control Circuit Schematic.

The main component for the volume controls the filters is the op-amp that controls the gain. The gain is calculated using Equation 2. Due to the second resister being a potentiometer, the gain can be changed. The goal is to have a maximum gain of -1 dB and a minimum gain of 0 dB. Thefore, the R_1 must be equal to 10 kΩ to be able to meet this requirement.

$$Gain = \frac{Vout}{Vin} = -\frac{R2}{R1}$$

$$-1 = -\frac{10\ k\Omega}{R1}$$

$$R4, R6, R7 = 10\ k\Omega$$

c. Main Voltage Control

After the filtered volume controllers, all the frequencies come back together into a summing amplifier to be able to control the master volume. The main volume control circuit shown in Figure 3.3.1 was constructed utilizing an LM324 chip with a initial resistance for each branch being 33 kΩ with a 10 kΩ potentiometer to control the gain of the op-amp for the second resistor. A +8 V and a -8 V travel through each LM324 with the voltages having a capacitor in parallel being grounded to prevent static from being amplified.

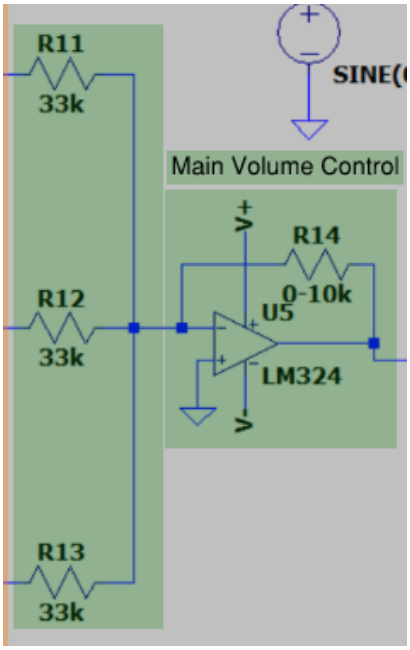

Figure 3.3.1: Main Volume Control Circuit Schematic.

The main component for the main volume controls the filters is the op-amp that controls the gain. The gain is calculated using Equation 2 and Equation 3 to convert V_{in} into V_{rms}. The input voltage to the circuit for each of the filters is $\frac{1}{2\sqrt{2}}$ V_{rms}, and the output voltage through each filter is with 0.1 V_{rms}. The input voltage comes from a 1 V_{pp} sin wave input that is then converted into V_{rms}. The output voltage is given as a requirement for the circuit. It is also known the second resister would be a potentiometer because of the need to be able to change the gain. Utilizing the known $V_{in,}$ V_{out}, and R_2, R_1 is able to be calculated to be ideally 35.4 kΩ. However, there is no 35.4 kΩ resistor, so a 33 kΩ resistor was used for each branch instead.

$$\text{Vin, rms} = \frac{V}{\sqrt{2}} = \frac{1\,Vpp}{\sqrt{2}} = \frac{\frac{1}{2}\,V}{\sqrt{2}} = \frac{1}{2\sqrt{2}}\,Vrms$$

$$Gain = \frac{Vout}{Vin} = -\frac{R2}{R1}$$

$$\frac{0.100\,Vrms}{\frac{1}{2\sqrt{2}}\,Vrms} = -\frac{10\,k\Omega}{R1}$$

$$R11, R12, R13 \ = 35.4\ k\Omega$$

d. Power Amplifier

After the main volume controllers, the voltage then travels through to the power amplifier. The power amplification circuit shown in Figure 3.4.1 was constructed utilizing an LM356 chip. A +8 V and a -8 V travel through each LM356 with the voltages having a capacitor in parallel being grounded to prevent static from being amplified.

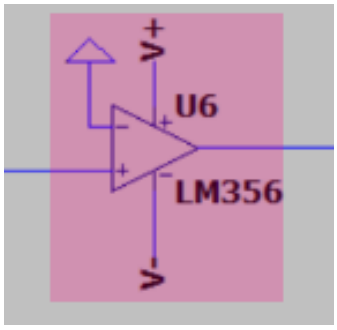

Figure 3.4.1: Main Volume Control Circuit Schematic.

The main component for the power amplifier is the op-amp that controls the gain. The power required to meet the circuit requirements uses Equation 4 and the gain that created by the power amplifier uses equation 3. The power required for the circuit must be at least 0.4 Watts and the speaker possesses a resistance of 8 Ω. Using Equation 4, the minimum voltage required to pass through the power amplifier needs to be 1.788 V. Using this output voltage, the gain can be calculated. The gain, therefore, should be at least 12.64 dB due to the op-amp.

$$\text{Power} = VI = \frac{V^2}{R} \Rightarrow V = \sqrt{PR}$$

$$V = \sqrt{(0.4\ W)(8\ \Omega)} = 1.788\ V$$

$$Gain = \frac{Vout}{Vin} = \frac{1.788\ V}{0.1\sqrt{2}\ V} = 12.64\ dB$$

e. Completed Circuit

Tying all the different circuit components together, the full circuit is created. The complete circuit shown in Figure 3.5.1 was constructed using the materials discussed previously. In total 4.7 kΩ resistors x3, 10 kΩ resistors x3, 33 kΩ resistors x3, 10 kΩ potentiometers x4, 0.01 µF capacitors x2, 0.1 µF capacitors x4, 100 µF capacitors x2 which is used for the speaker, LM 324 chips x5 (technically could do it in 2 but a maximum of 5 is needed), LM 356 chip x1, 8 V DC for chips, -8 V DC for chips, and an input AC voltage.

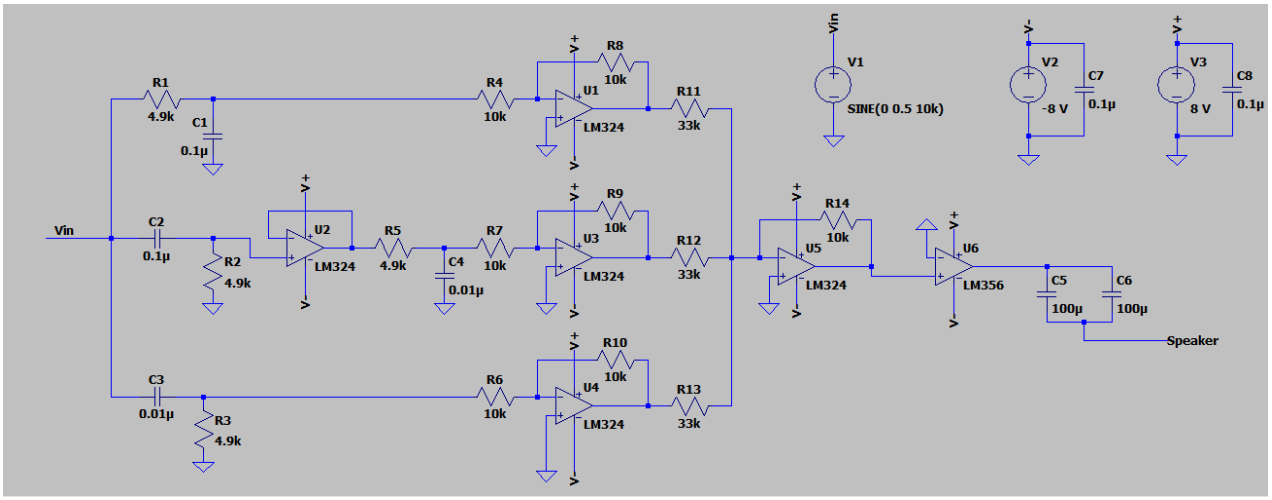

Figure 3.5.1: Complete Circuit Schematic

4. Results

To test if the cutoff requirement for the low-pass filter was effective, a frequency analysis was performed. It would test the gain of the circuit when different frequencies passed through the circuit. The cutoff should take place at -3 dB with a frequency of 320 Hz. Shown in Figure 4.1 the cutoff was -2.97 dB with a frequency of 324.7 Hz. The gain % error was 1% and the frequency % error was 1.47% as shown in Table 4.1.

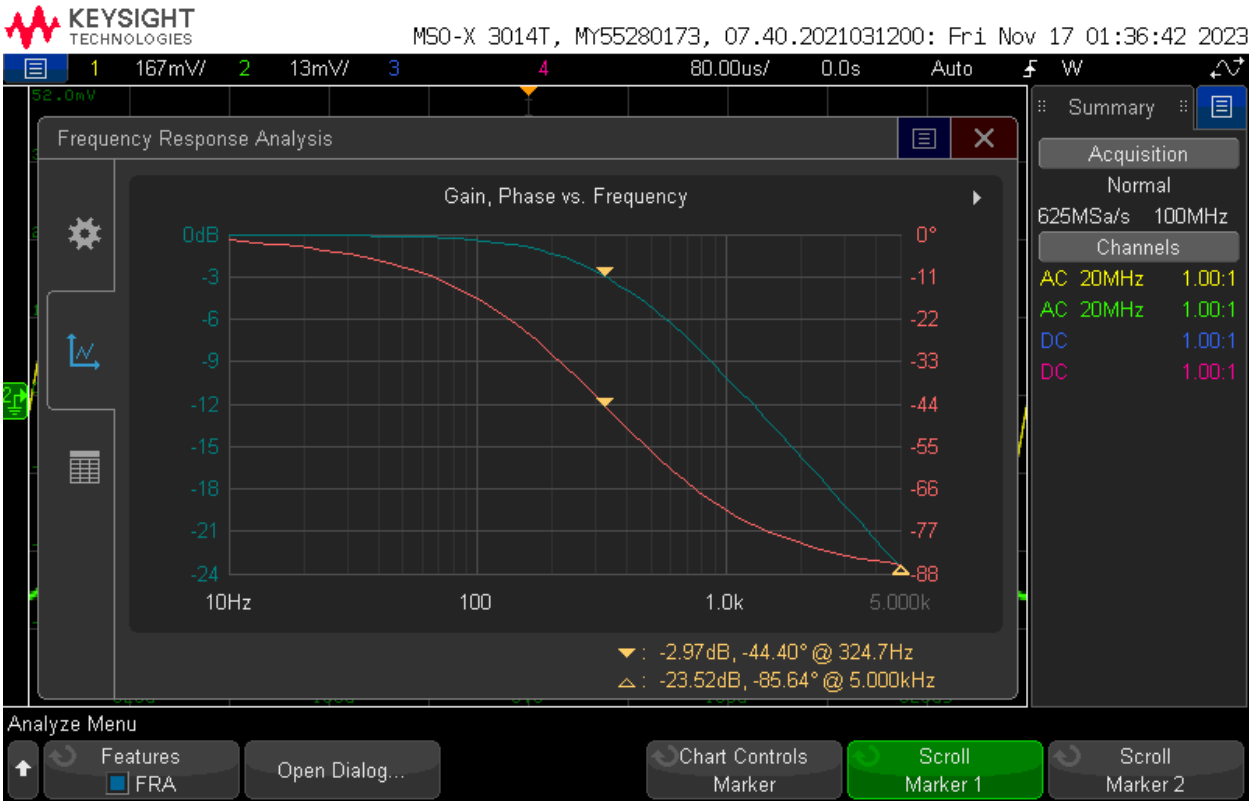

Figure 4.1: Low-Pass Filter Gain vs Frequency.

Table 4.1: Low-Pass Filter Gain vs Frequency Results.

	Results	Units
Theoretical Gain	-3.00	dB
Experimental Gain	-2.97	dB
Gain % Error	1.00	%
Theoretical Frequency	320.00	Hz
Experimental Frequency	324.70	Hz
Frequency % Error	1.47	%

To test if the cutoff requirement for the high-pass filter was effective, a frequency analysis was performed. It would test the gain of the circuit when different frequencies passed through the circuit. The cutoff should take place at -3 dB with a frequency of 3200 Hz. Shown in Figure 4.2 the cutoff was -3.13 dB with a frequency of 3311 Hz. The gain % error was 4.33% and the frequency % error was 3.47% as shown in Table 4.2.

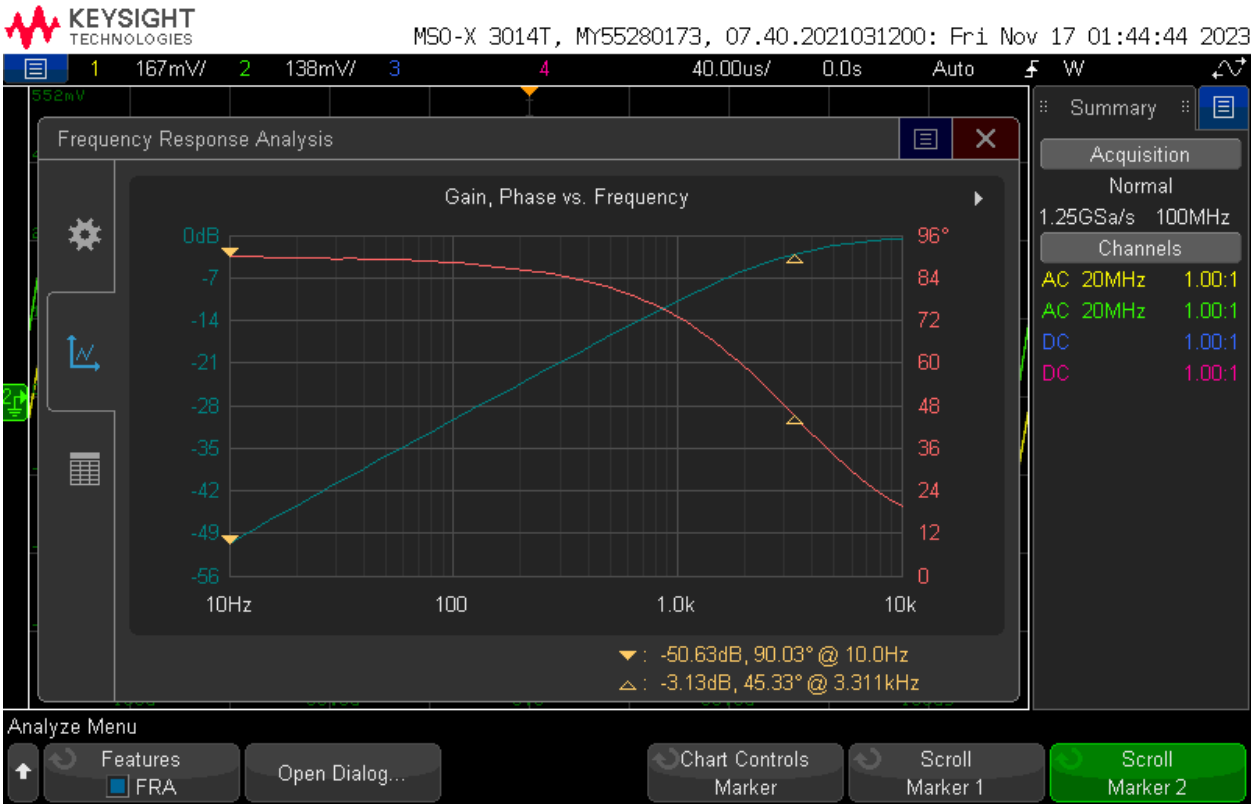

Figure 4.2: High-Pass Filter Gain vs Frequency.

Table 4.2: High-Pass Filter Gain vs Frequency Results.

	Results	Units
Theoretical Gain	-3.00	dB
Experimental Gain	-3.13	dB
Gain % Error	4.33	%
Theoretical Frequency	3200.00	Hz
Experimental Frequency	3311.00	Hz
Frequency % Error	3.47	%

To test if the cutoff requirement for the mid-pass filter was effective, a frequency analysis was performed. It would test the gain of the circuit when different frequencies passed through the circuit. The cutoff should take place at -3 dB with a frequency of 320 Hz and 3200 Hz. Shown in Figure 4.3 the cutoff was -3.20 dB with a frequency of 316.2 Hz and -3.05 dB with a frequency of 3162 Hz. The gain % error was 6.67% and 1.67% while the frequency % error was 1.19% and 1.19% as shown in Table 4.2.

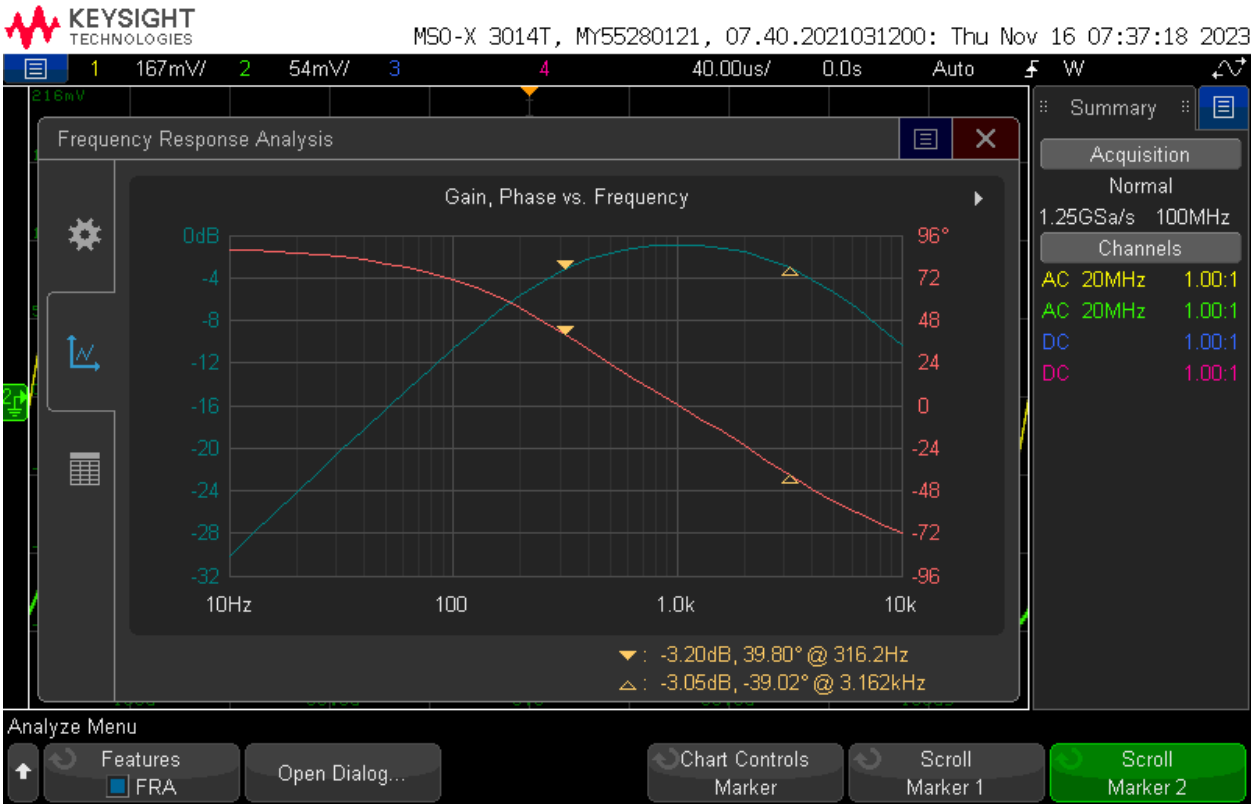

Figure 4.3: Mid-Pass Filter Gain vs Frequency.

Table 4.3: Mid-Pass Filter Gain vs Frequency Results.

	Results	Units
Theoretical Gain	-3.00	dB
Experimental Gain High Pass	-3.20	dB
Experimental Gain Low Pass	-3.05	dB
Low Pass Gain % Error	6.67	%
High Pass Gain % Error	1.67	%
Theoretical Frequency High Pass	320.00	Hz
Experimental Frequency High Pass	316.20	Hz
Theoretical Frequency Low Pass	3200.00	Hz
Experimental Frequency Low Pass	3162.00	Hz
High Pass Frequency % Error	1.19	%
Low Pass Frequency % Error	1.19	%

The next element to test is V_{amp} with all volumes turned to the minimum settings. This was done at 3 different frequencies, 200 Hz, 2000 Hz, and 10000 Hz. The reason for 3 different frequencies is because of the different filters take place. By using different frequencies, it shows that each of the filters is effective. The corresponding graphs can be seen in Figure 4.4, Figure 4.5, and Figure 4.6 with Table 4.2 showing the results in a clear manner. The circuit requirement calls for V_{amp} to not exceed 15 mV for DC rms. It can be seen in the results that the circuit was able to achieve this for each of the different frequencies.

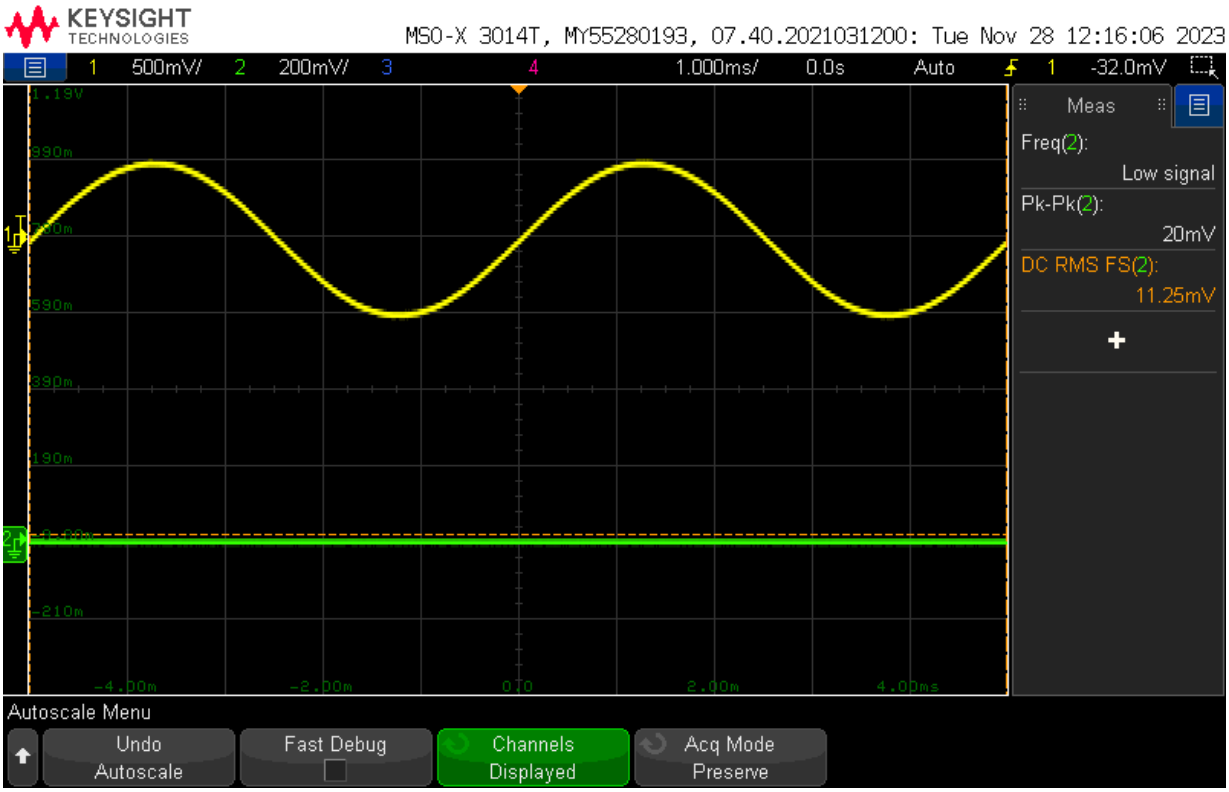

Figure 4.4: V_{amp} at 200 Hz with Minimum Settings.

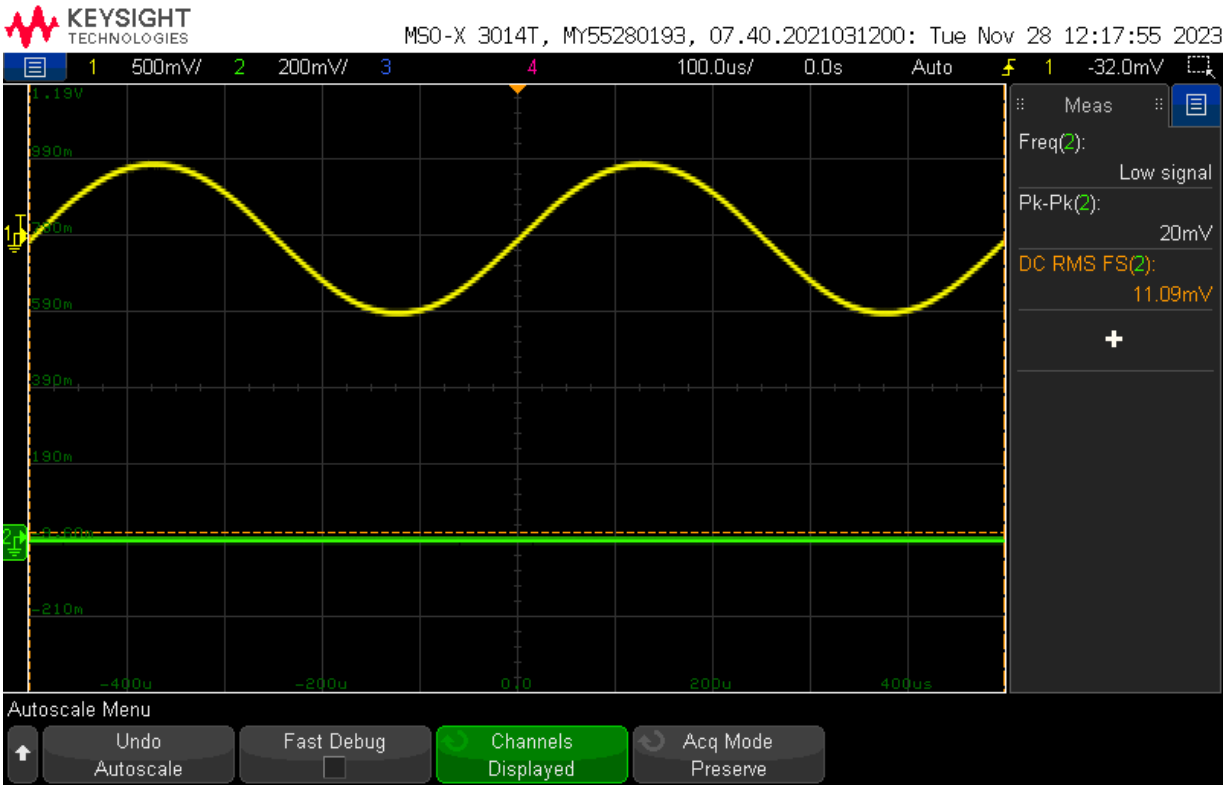

Figure 4.5: V_{amp} at 2000 Hz with Minimum Settings.

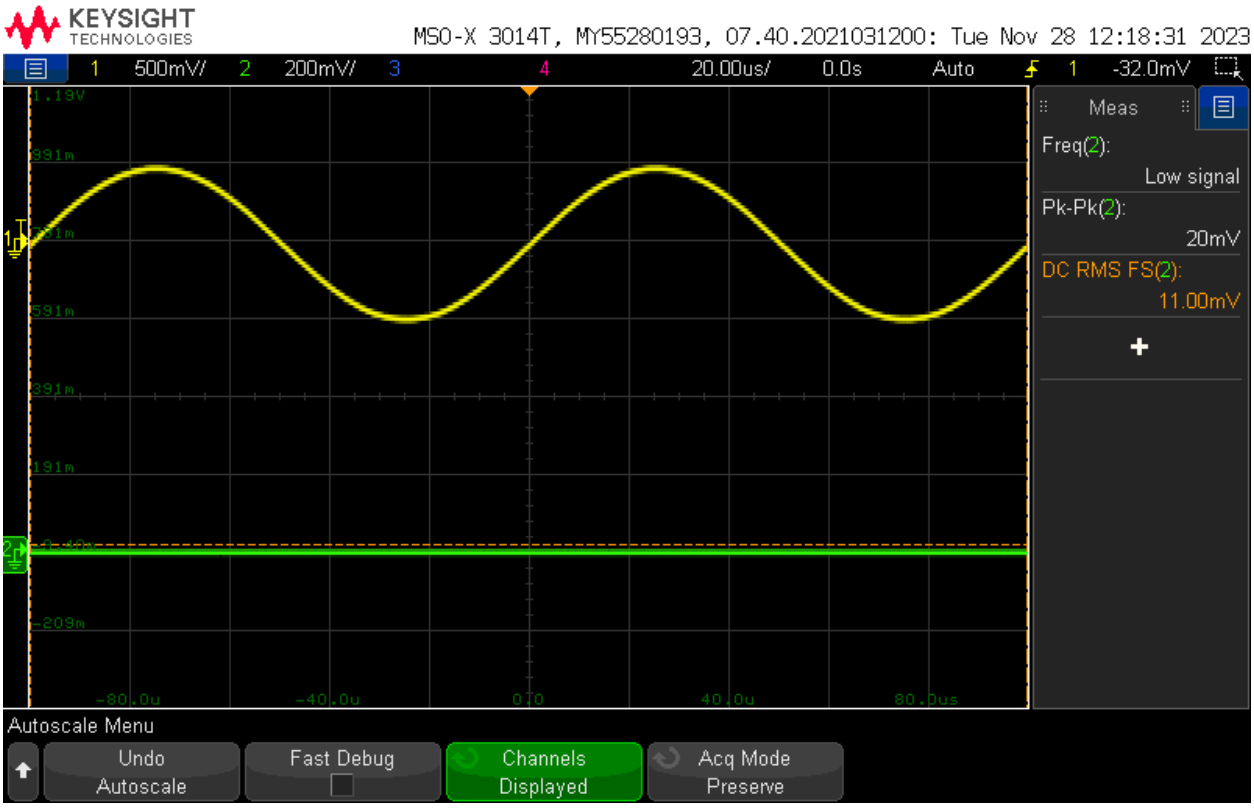

Figure 4.6: V_{amp} at 10000 Hz with Minimum Settings.

Table 4.4: V_{amp} at Different Frequencies with Minimum Settings Results.

Frequency (Hz)	Maximum RMS Voltage (mV)	DC RMS Voltage (mV)
200	15.00	11.25
2000	15.00	11.09
10000	15.00	11.00

After testing for the minimum setting, it was time to test V_{amp} at maximum settings. Testing at 3 different frequencies was preformed, 200 Hz, 2000 Hz, and 10000 Hz. The reason for 3 different frequencies is because of the different filters take place. By using different frequencies, it shows that each of the filters is effective. The corresponding graphs can be seen in Figure 4.7, Figure 4.8, and Figure 4.9 with Table 4.3 showing the results in a clear manner. The circuit requirement calls for V_{amp} to be 100 mV for DC rms with a % error of $\pm$10%. It was found that the circuit was not able to meet this requirement for 200 Hz and 2000 Hz having a DC rms of 85.4 mV and 85.2 mV respectively. This exceeds the 10% error margin. A possible reason for this is due to the low pass filter using 0.1 µF. The reason for this claim is because it is the only element that the low-pass filter and mid-pass filter share that is also different from the similarities to the high-pass filter. The values are so close together that it feels unlikely to be related to the tolerances of the resistors too.

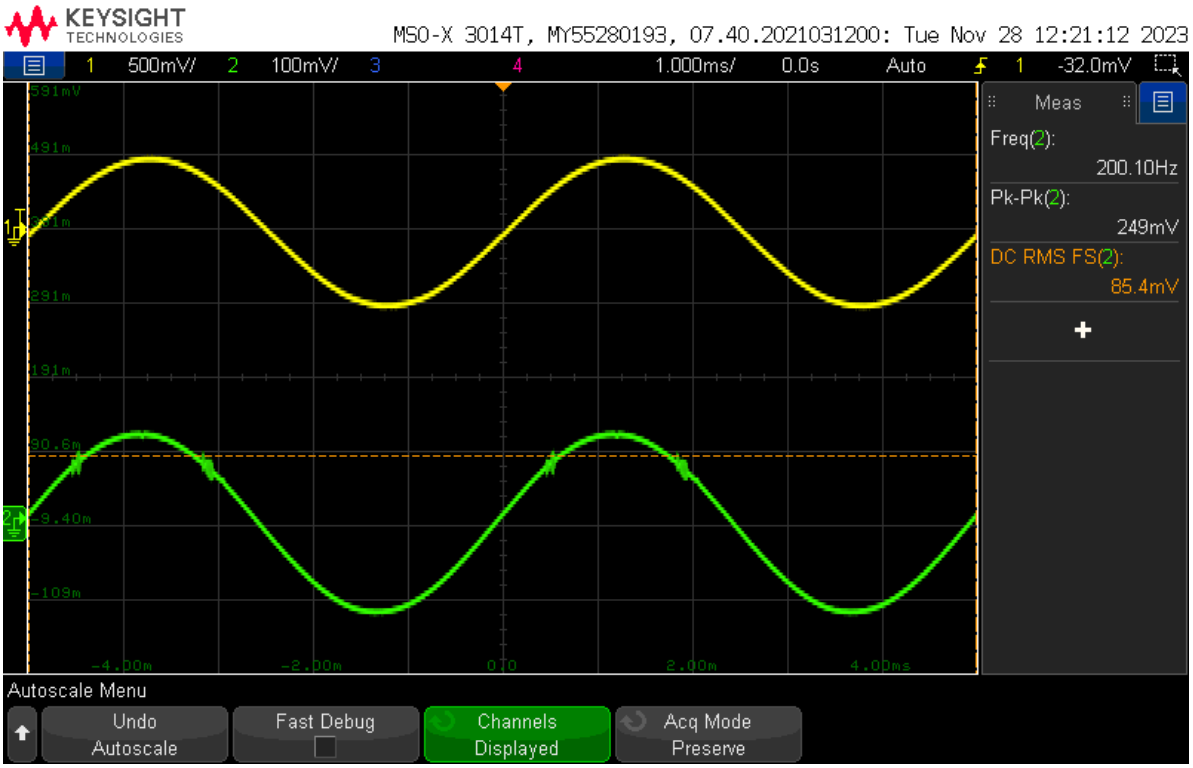

Figure 4.7 V_{amp} at 200 Hz with Maximum Settings.

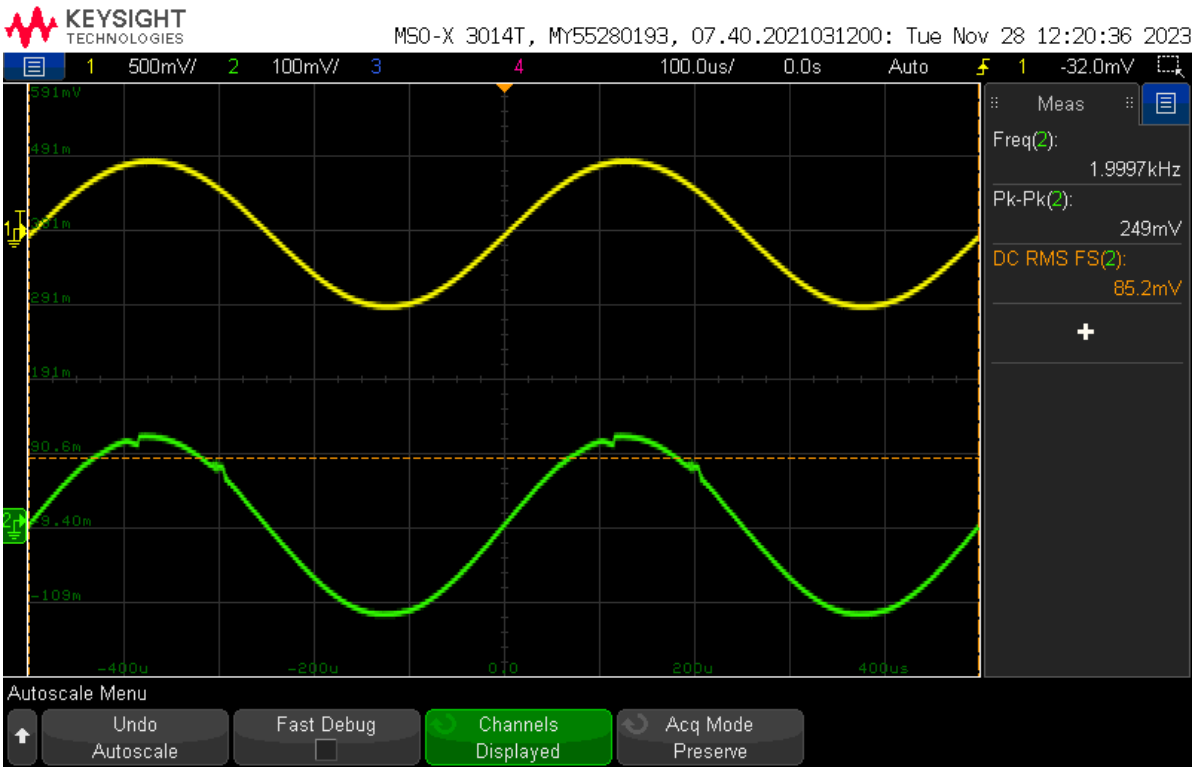

Figure 4.8: V_{amp} at 2000 Hz with Maximum Settings.

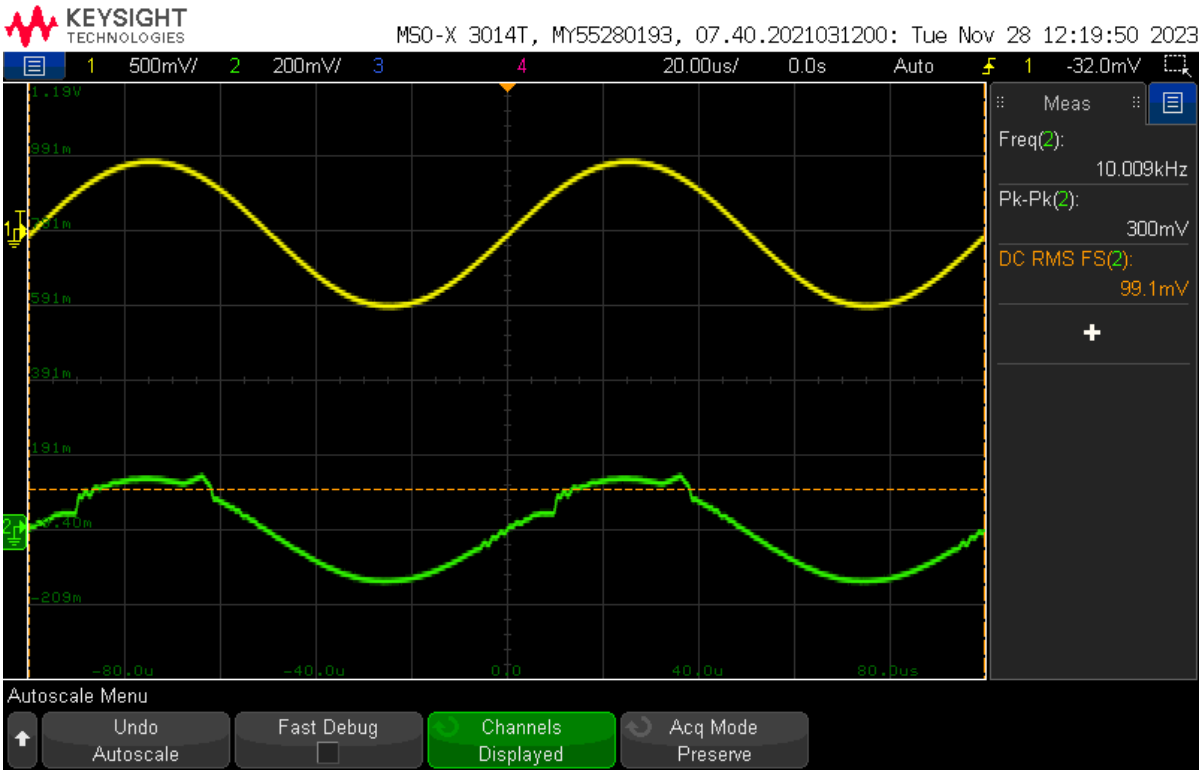

Figure 4.9: V_{amp} at 10000 Hz with Maximum Settings.

Table 4.5: V_{amp} at Different Frequencies with Maximum Settings Results.

Frequency (Hz)	Theoretical RMS Voltage (mV)	DC RMS Voltage (mV)	RMS % Error (%)
200	100.00	85.40	14.60
2000	100.00	85.20	14.80
10000	100.00	99.10	0.90

After testing for the maximum setting, the ripple throughout the circuit was tested. This was completed by performing a gain vs frequency experiment through the whole circuit before it reaches the power amplifier. After performing a gain vs frequency experiment, the point when the gain is the greatest and the least was tested to find the DC rms voltage. The greatest gain was at 10000 Hz with a gain of -10.78 dB. The DC rms voltage was found to be 98.9 mV. The lowest gain was at 200 Hz with a gain of -12.30 dB. The DC rms voltage was found to be 85.5 mV. The requirement for the circuit is that the difference between the two voltages could not exceed 15 mV. The difference found was 13.4 mV which meets the requirement for the circuit.

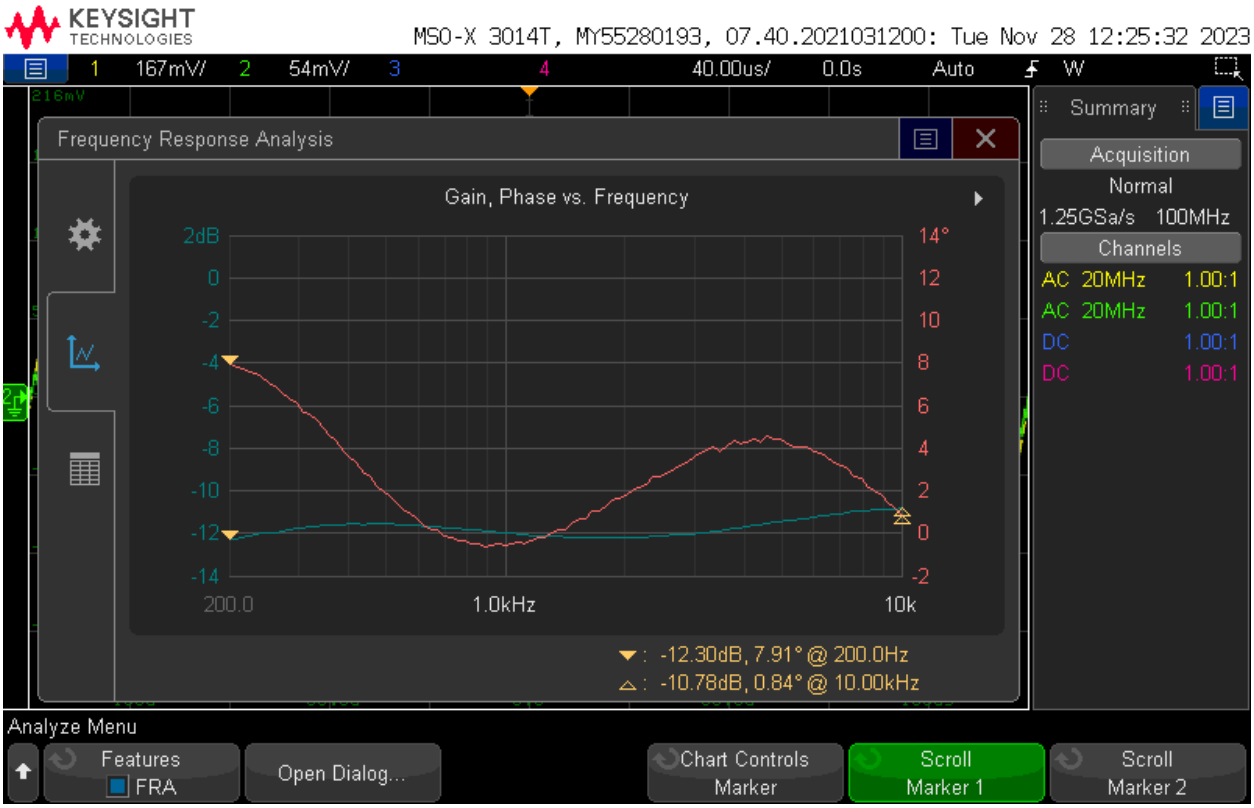

Figure 4.10: V_{max} - V_{min} Gain vs Frequency.

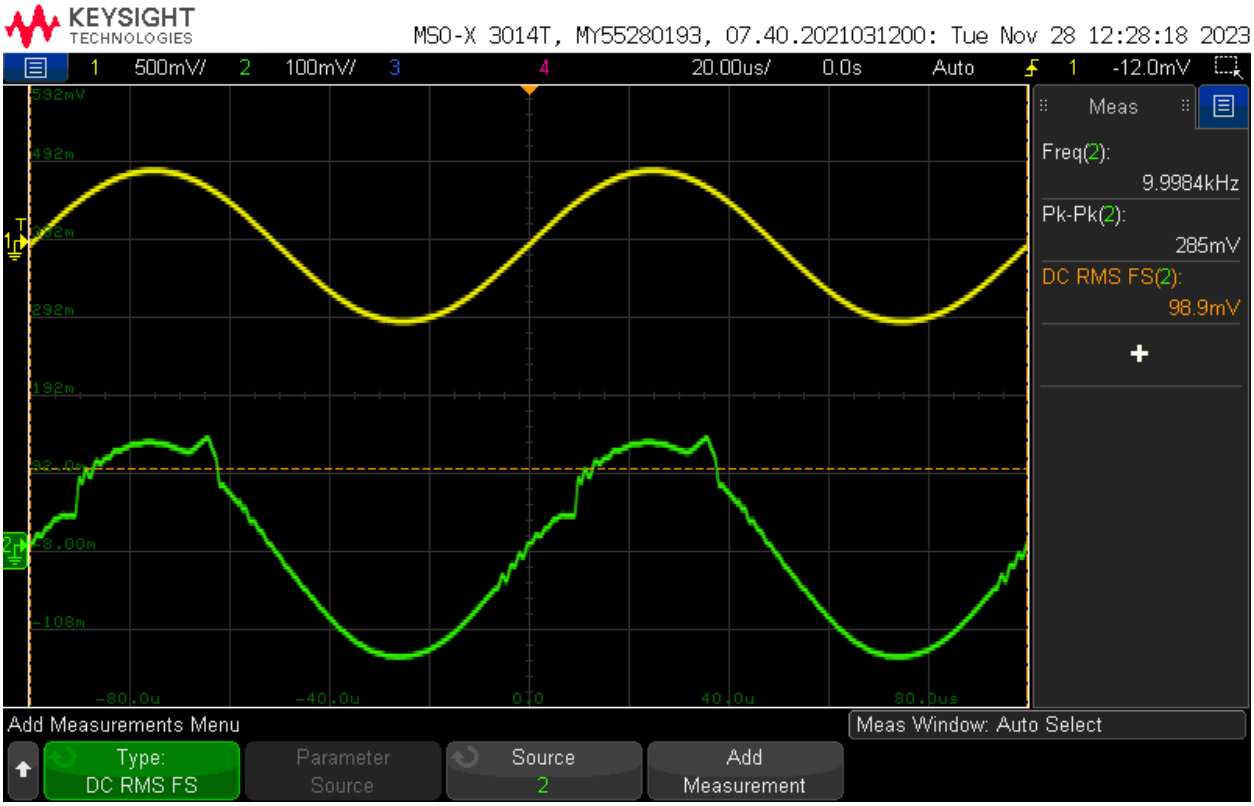

Figure 4.11: V_{max} DC RMS Value.

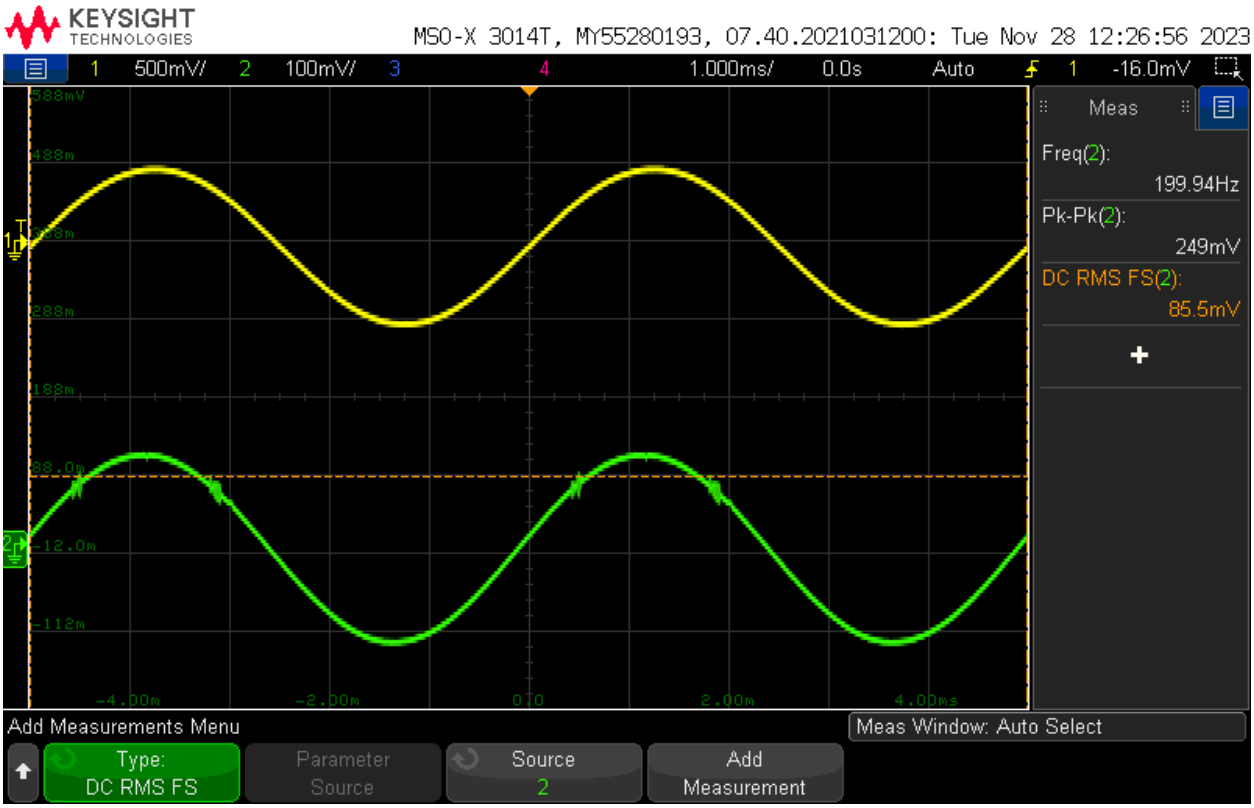

Figure 4.12: V_{min} DC RMS Value.

Table 4.6: V_{max} - V_{min} RMS Voltage Difference Results.

Frequency (Hz)	DC RMS Voltage (mV)	Maximum RMS Voltage Difference(mV)	DC RMS Voltage Difference (mV)
10000	98.90	15.00	13.40
200	85.50		

After testing for the ripple, the amplifier output power throughout the circuit was tested. This was completed by performing a gain vs frequency experiment through the whole circuit. After performing a gain vs frequency experiment, the point when the gain is the least was tested to find the DC rms voltage. The lowest gain was at 200 Hz with a gain of 14.54 dB. The DC rms voltage was found to be 1.90 V. The 1.90 V was then used in Equation 4 to find that the power was 0.451 Watts, which is greater than the circuit requirement of 0.4 Watts. Additionally, the theoretical gain was found to be 12.64 dB, but the smallest gain was found to be 14.54 dB. That is an error of 15%. A possible reason for this error is due to the error of the maximum V_{amp} causing the error to then continue through the circuit, being amplified through the op-amps.

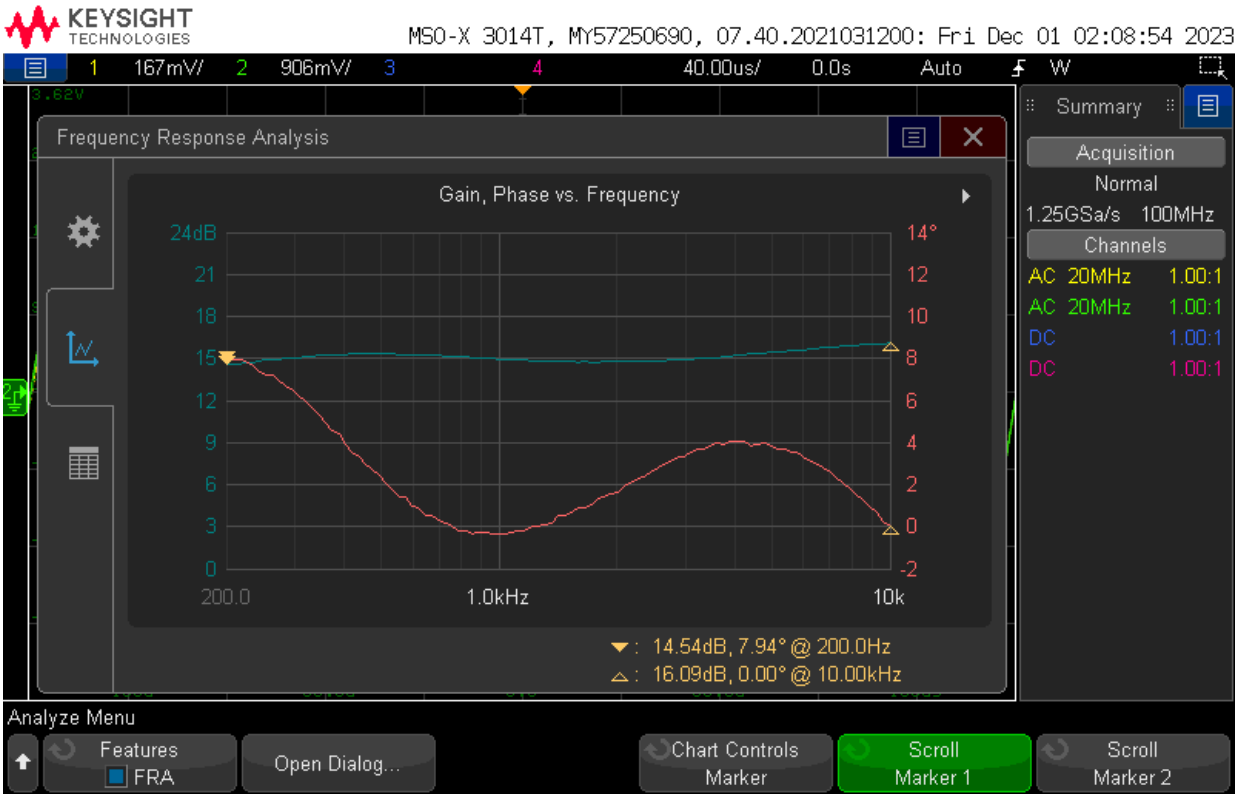

Figure 4.13: Minimum Gain Through Power Amplifier.

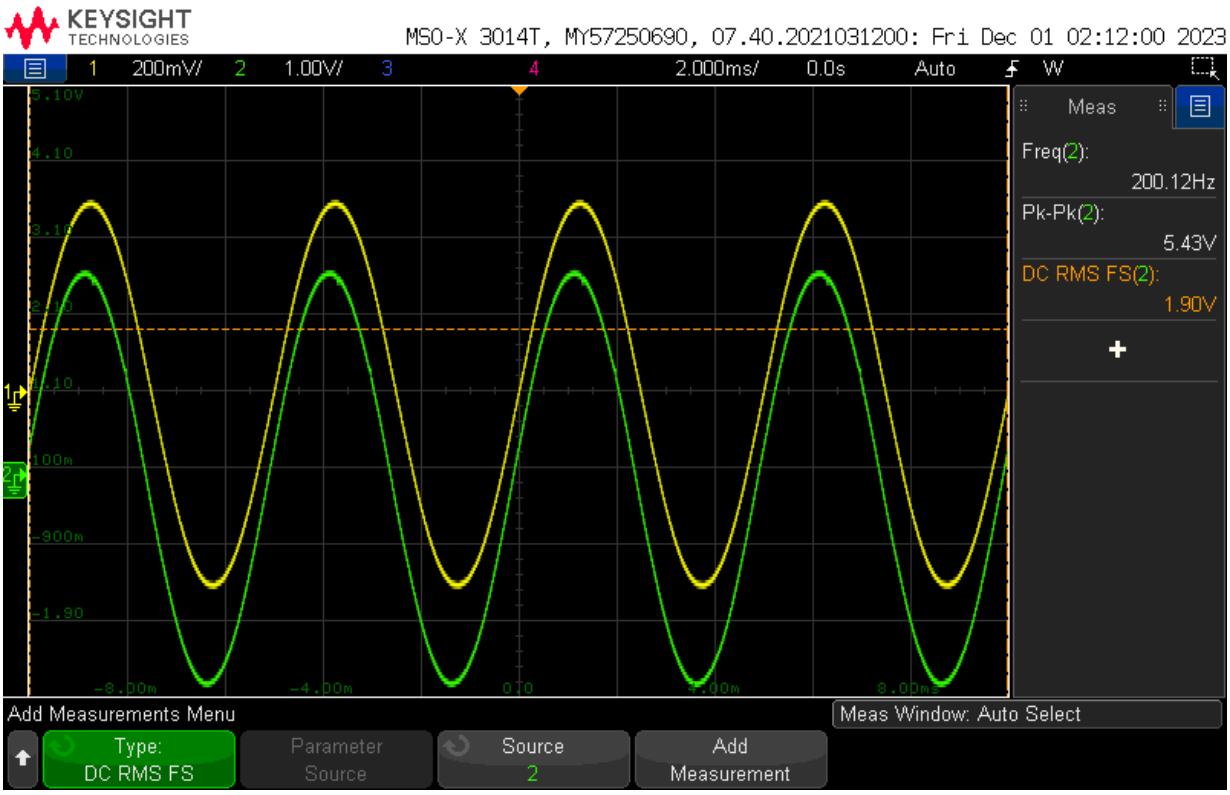

Figure 4.14: DC RMS Voltage Out of Power Amplifier at 200 Hz.

Table 4.7: Circuit DC RMS Voltage Results.

Minimum DC Voltage (V)	Experimental DC Voltage (V)	% Error (%)
1.788	1.90	6.26

$$\text{Power} = VI = \frac{V^2}{R} = \frac{(1.9\ V)^2}{8\ \Omega} = 451\ mW$$

Table 4.8: Power Amplifier Gain Results.

Theoretical Gain (dB)	Experimental Gain (dB)	% Error (%)
12.64	14.54	15.03

As a final test, music was played through the circuit. The circuit was able to provide clear audio with adjustability from the potentiometers to control the volume of each frequency range as well as the overall volume.

5. Conclusion

The primary object of this experiment was to design and create an audio equalizer, whilst completing the constraints detailed in Figure 1.1. The key goals involve implementing a low-pass filter, a mid-pass filter, and a high-pass filter with individual volume controls that possess a specific cutoff frequency of 320 Hz, 320-3200 Hz, and 3200 Hz respectively. Additional goals are having V_{amp} with minimum settings having less than 15 mV_{rms} all frequencies and having V_{amp} with maximum settings having 100 mV_{rms} all frequencies with an error of 10%. Furthermore, the maximum ripple needs to be 15 mV_{rms} and the output power needs to be greater than 400 mW for all frequencies.

The method to complete these requirements was by breaking the complete circuit down into smaller elements. Each of the filters were separated and tested before completing the whole process.

After the analysis of the circuit a few key findings were determined. Frequency analyses were conducted to evaluate the performance of the low-pass, mid-pass, and high-pass filters. The results of the filters are close to the theoretical cutoff frequencies. Additionally, the V_{amp} testing at both minimum and maximum settings showed control of volume levels at various frequencies.

There was a shortcoming with the circuit. While the circuit performed well in maintaining cutoff frequencies and volume control, the circuit failed to meet the maximum V_{amp} requirement at certain frequencies. At 200 Hz and 2000 Hz, the DC RMS voltages exceeded the 10% margin of error. This is most likely due to the selection of low-pass filter capacitors.

Overall, the experiment largely met its object. A successfully designed audio equalizer with functional filters, volume controls, and power amplification was constructed. Despite minor shortcomings from the maximum V_{amp}, the circuit's overall performance was acceptable. Adjustments to component values may be considered in the future if the circuit were to be reconstructed.